DETAILED ACTION

REASONS FOR ALLOWANCE

1. Claims 10, 14, 15, 45 – 51 and 54 – 58 are allowed.

2. The following is an examiner's statement of reasons for allowance:

The prior art of record does not teach or suggest, either singularly or in combination, at least a contact structure of a wire comprising an Al-based material wire on a substrate; an inter-layer reaction layer; a conductive layer directly connected to the wire via the inter-layer reaction layer, wherein the wire is a gate wire and includes a gate line, a gate electrode connected to the gate line, and a gate pad which is connected to the gate line and receives a signal from an external circuit (claim 1) and wherein the first wire is a data wire and includes a data line, a source electrode connected to the data line, a drain line, a drain electrode which is separated from the source electrode and opposite to the source electrode with respect to the gate electrode, and a data pad which is connected to the data line and receives a signal from an external circuit (claim 51). Sakata et al. (U. S. Pat. No. 6,252,247) teaches a contact structure of a wire comprising an Al-based material wire on a substrate; an inter-layer reaction layer; a conductive layer directly connected to the wire via the inter-layer reaction layer. However, Sakata et al. does not teach the wire being a gate wire and including a gate line, a gate electrode connected to the gate line, and a gate pad which is connected to the gate line and receives a signal from an external circuit as set forth in claim 1 and wherein the first wire is a data wire and includes a data line, a source electrode connected to the data line, a drain line, a drain electrode which is separated from the source electrode and opposite to the source electrode with respect to the gate electrode, and a

data pad which is connected to the data line and receives a signal from an external circuit as set forth in claim 51.

Furthermore for the claim 45, the prior art of record does not teach or suggest, either singularly or in combination, at least a thin film transistor array panel comprising a gate wire … includes a gate line, a gate insulating layer, a semiconductor layer, a data wire … includes a data line, a passivation layer, an inter-layer reaction layer, a transparent conductive layer pattern electrically connected to the gate wire or the data wire through a contact hole of the gate insulating layer or the passivation layer and wherein the transparent conductive layer pattern is electrically connected to the gate wire to the data wire via the inter-layer reaction layer. Sakata et al. (U. S. Pat. No. 6,252,247) teaches a thin film transistor array panel comprising a gate wire, a gate insulating layer, a semiconductor layer, a passivation layer, an inter-layer reaction layer, a transparent conductive layer pattern electrically connected to the gate wire or the data wire through a contact hole of the gate insulating layer or the passivation layer and wherein the transparent conductive layer pattern is electrically connected to the gate wire to the data wire via the inter-layer reaction layer. However, Sakata et al. does not teach a thin film transistor array panel comprising a gate wire … includes a gate line, a data wire … includes a data line, and wherein the transparent conductive layer pattern is electrically connected to the gate wire to the data wire via the inter-layer reaction layer as set forth in claim 45.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRIS C. CHU whose telephone number is (571)272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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